

FIG. 1

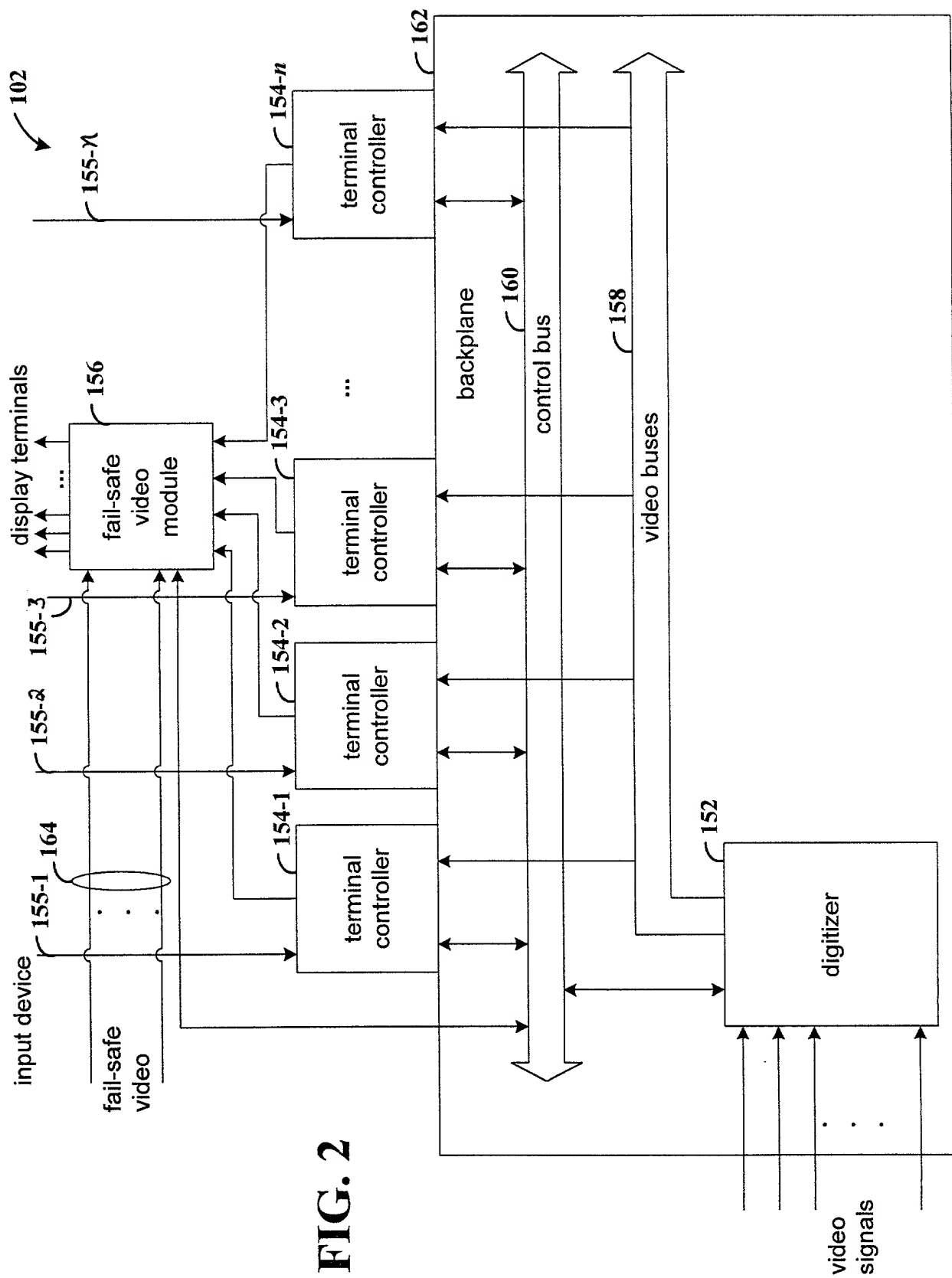


FIG. 2

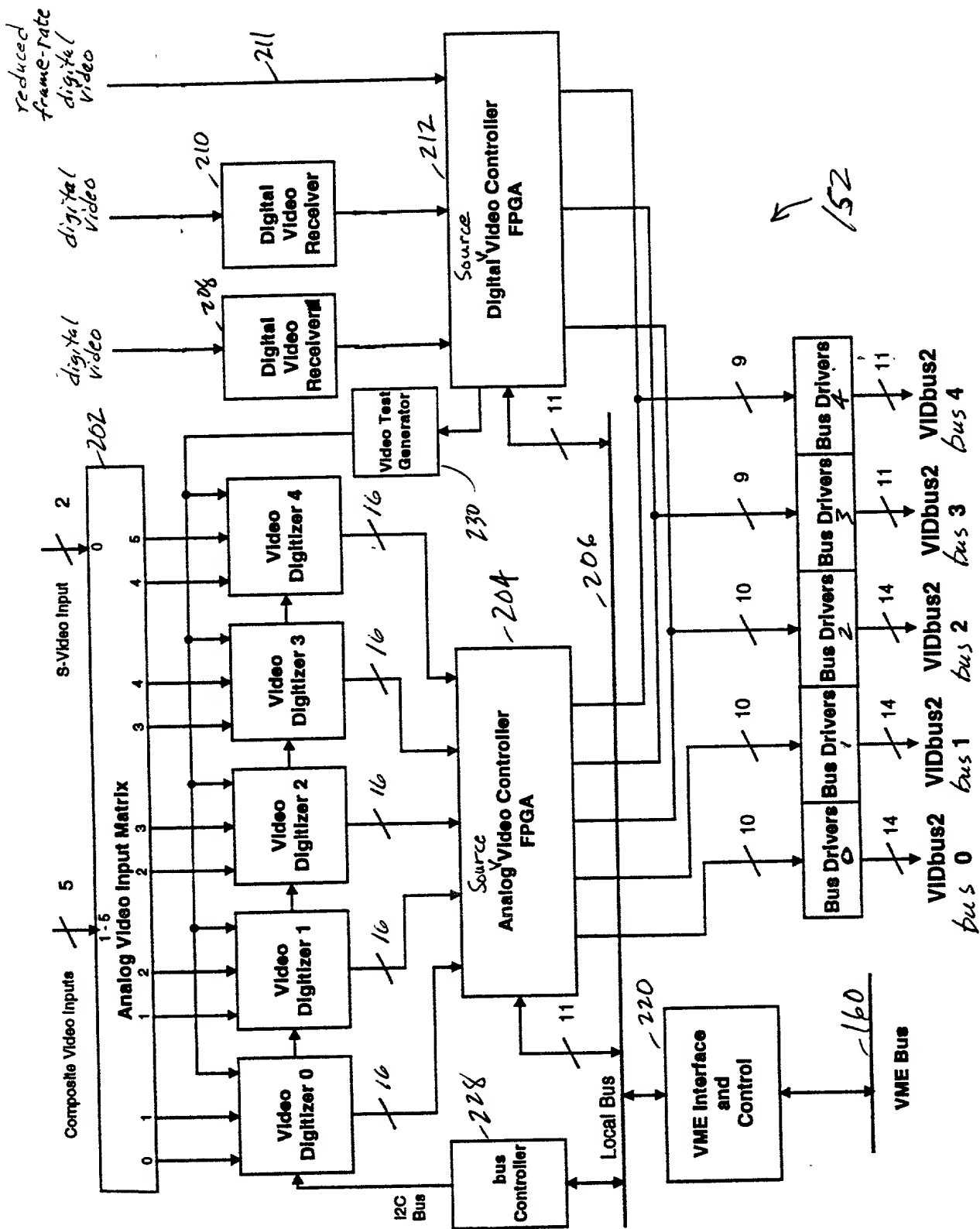


FIG. 3

The diagram illustrates the system architecture for video processing. At the top, two inputs are labeled "fail-safe video" and "terminal controllers". The "fail-safe video" input is connected to a "multiplexer and relay module" via a 164-bit bus. The "terminal controllers" input is connected to the same module via a 252-bit bus. The "multiplexer and relay module" is connected to the "VME INTERFACE AND CONTROL LOGIC" block via a 256-bit bus. The "VME INTERFACE AND CONTROL LOGIC" block is connected to the "fail-safe video" input via a 156-bit bus. The "VME INTERFACE AND CONTROL LOGIC" block is also connected to the "terminal controllers" input via a 10-bit bus. The "VME INTERFACE AND CONTROL LOGIC" block is connected to the "multiplexer and relay module" via an 8-bit bus. The "VME INTERFACE AND CONTROL LOGIC" block is connected to the "fail-safe video" input via a 271-bit bus. The "VME INTERFACE AND CONTROL LOGIC" block is connected to the "terminal controllers" input via a 270-bit bus. The "multiplexer and relay module" outputs four video signals labeled "RGB VIDEOS OUT" with bit widths of 254, 256, and 258 bits.

FIG. 4

00547"6436/50

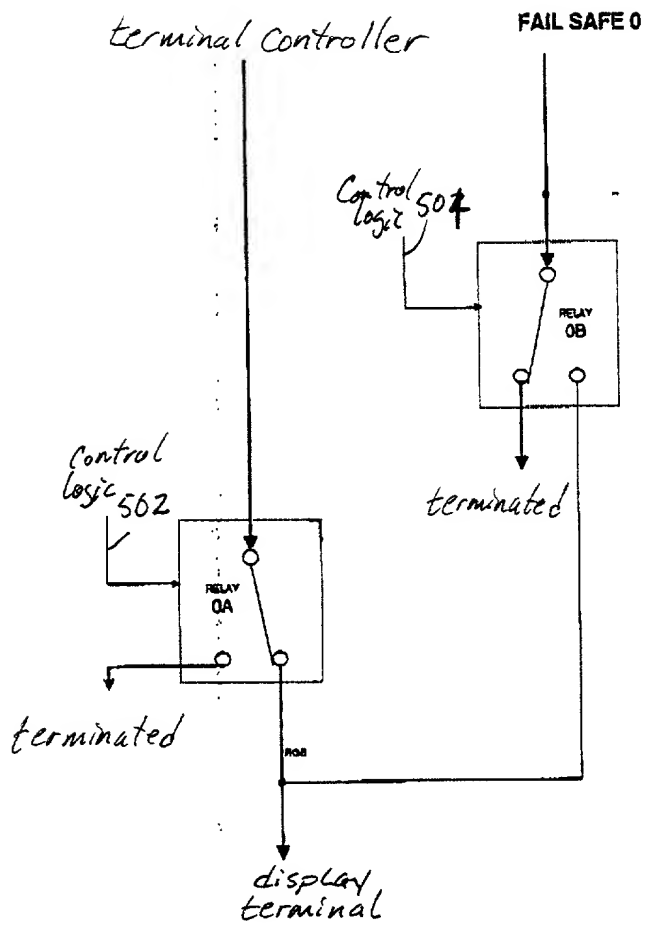


FIG. 5

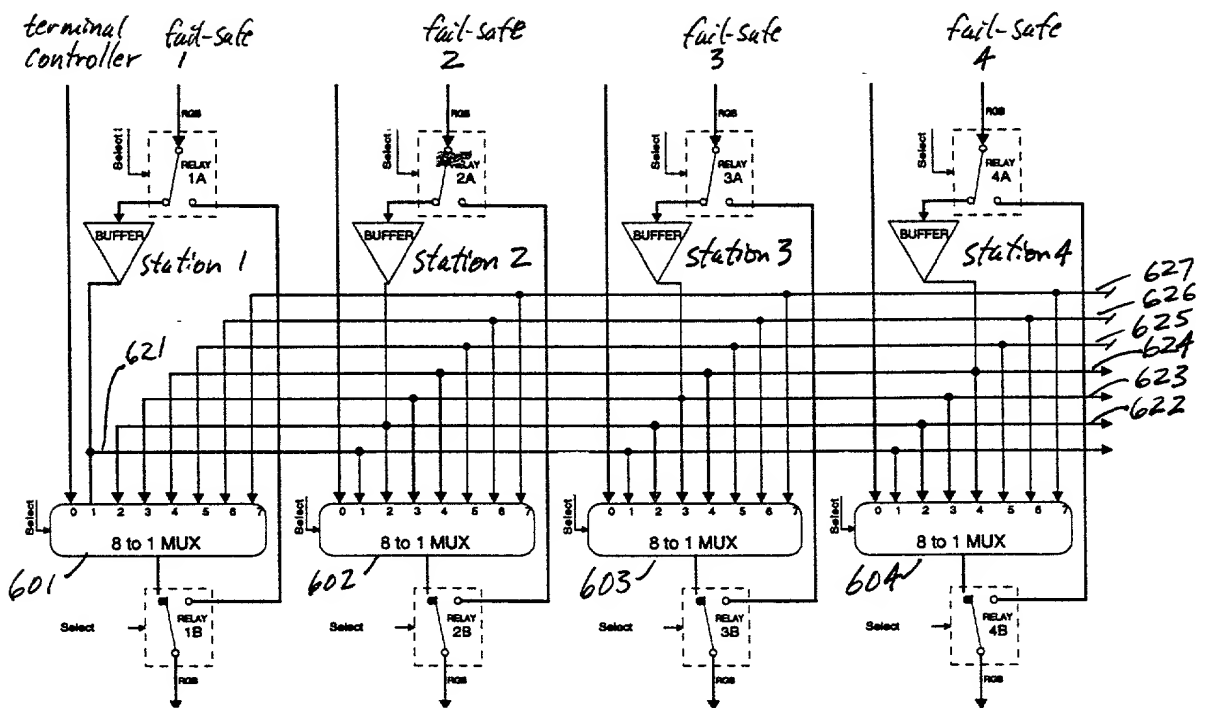


FIG. 6A

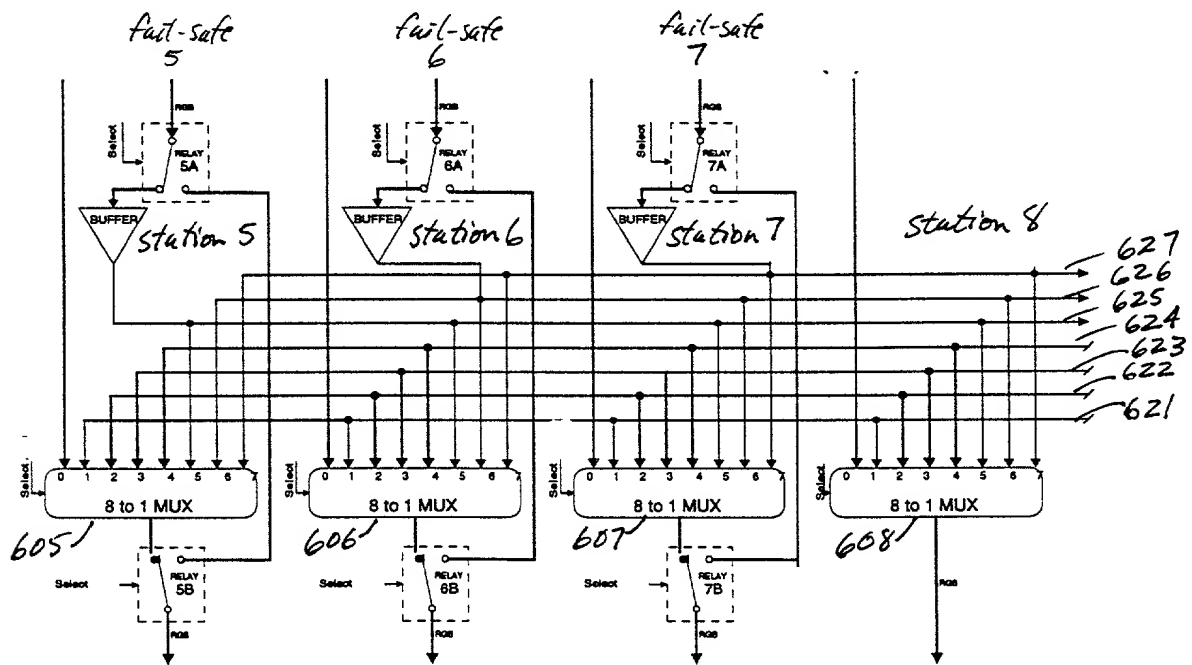


FIG. 6B